

SYSTEMS AND METHODS FOR SWITCHING TO A BACK-UP POWER SUPPLY

FIELD OF THE INVENTION

5 This invention relates in general to providing a back-up power supply, and more specifically to systems and methods for switching to a back-up power supply.

DESCRIPTION OF THE RELATED ART

10 Much of today's electronic equipment needs a constant power source. When a power supply fails, the switch to a backup supply should be instantaneous such that the load voltage does not dip below a set threshold. Typically diodes are used in an "OR" configuration (i.e. either the main supply or the backup supply delivers power to the load). Many applications, however, have tight voltage tolerances, and the loss through a diode is too great. Therefore, there exists a need for systems and methods
15 for addressing these and/or other problems related to providing a back-up power supply.

BRIEF DESCRIPTION OF THE DRAWINGS

20 The invention can be better understood with reference to the following drawings. The components in the drawings are not necessarily drawn to scale, emphasis instead being placed upon clearly illustrating the principles of the present invention. In the drawings, like reference numerals designate corresponding parts throughout the several views.

25 FIG. 1 is a block diagram depicting a power-switching circuit according to an embodiment of the invention.

 FIG. 2A is a block diagram depicting an example of the threshold detector shown in FIG. 1.

 FIG. 2B is a graph illustrating a non-limiting example of a transient hysteresis effect within the threshold detector shown in FIG. 2A.

30 FIG. 3 is a block diagram depicting an example of the inverter shown in FIG. 1.

FIG. 4 is a block diagram depicting an example of an inverting switch shown in FIG. 1.

FIG. 5 is a block diagram depicting an example of a power switch shown in FIG. 1.

5 FIG. 6 is a block diagram depicting an example of a voltage supply circuit.

FIG. 7 is a flow chart depicting a method according to one embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

10 An embodiment of the invention enables sustained power to DC-input end-use electronics. The embodiment is useful in applications that have primary and backup power sources. If the primary source fails, then the backup source is supplied to the load instead of the primary source. Switches used in this embodiment are very low loss and can pass high currents to the load with very little drop in voltage.

15 A condition for switching between one source and another is a voltage level of the primary source (V_p). If V_p falls below a threshold set by a comparison circuit, then the load is powered by the back-up power supply. Conversely, if V_p rises above the threshold, then the load is powered by the primary power supply.

Low resistance field effect transistors (FETs) may be used as switches, and
20 may be controlled by a threshold detection circuit. Using FETs enables a commercial “off the shelf” power source to be used, without the need to have a higher voltage source to overcome diode losses.

Below is a detailed description of the accompanying 6 figures, which illustrate a preferred embodiment of the present invention: FIG. 1 depicts an embodiment of a
25 power-switching circuit; FIGS. 2-5 depict examples of components of the power-switching circuit; and FIG. 6 depicts an example of a voltage supply circuit. Note, however, that the invention may be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Furthermore, all examples given herein are intended to be non-limiting, and are provided in order to
30 help clarify the description of the invention.

FIG. 1 is a block diagram depicting a power-switching circuit 100 according to an embodiment of the invention. The power-switching circuit 100 may be used in many electronic devices that require a constant DC power source. As a non-limiting

example, among others, the power-switching circuit 100 may be used in an up-converter device configured to increase the frequency of a signal.

As shown in FIG. 1, the power-switching circuit 100 includes a threshold detector 102 that is coupled to voltages V_B and V_P . The threshold detector 102 compares the voltage V_B and the voltage V_P and is operative to turn on or off an inverting switch 106-1 and an inverting switch 106-2 responsive to whether the voltage V_B and the voltage V_P are within a predetermined value. The inverting switch 106-1 and the inverting switch 106-2 are configured to turn on and off in a complementary manner. In other words, when the inverting switch 106-1 is turned on, the inverting switch 106-2 is turned off and vice-versa.

The inverter 104 enables the inverting switch 106-1 to act in a complementary manner to the inverting switch 106-2. In an alternative embodiment the inverter 104 may be coupled between the threshold detector 102 and the inverting switch 106-2. In a preferred embodiment, the inverting switch 106-1 and the inverting switch 106-2 are turned off at a time period set by R12 and C2 of figure 4, after a corresponding change in the output of the threshold detector 102. Such a time period may vary between a few microseconds to over 100 milliseconds, depending on the values of R12 and C2. In one embodiment, among others, the time period may be 30 milliseconds. This delayed switching is implemented in order to maintain a constant voltage output of the power-switching circuit 100.

The inverting switch 106-1 and the inverting switch 106-2 are coupled to a back-up power switch 108-1 and to a primary power switch 108-2, respectively. The back-up power switch 108-1 and the primary power switch 108-2 may be coupled to the voltage V_B and the voltage V_P , respectively.

When 100 is in operation, the voltage V_O is substantially equal to the voltage V_P if the voltage V_P is within a certain threshold, otherwise the voltage V_O is equal to the voltage V_B . In this manner, when a primary power source fails, a backup power source may be provided to a load.

FIG. 2A is a block diagram depicting an embodiment of the threshold detector 102 shown in FIG. 1. The threshold detector 102 receives primary voltage V_P and back-up voltage V_B as inputs and provides voltage V_3 as an output. The threshold detector 102 includes a comparator A_1 which receives inputs via the connections 201 and 202, and provides an output via a connection 206. The connection 201 is coupled

to nodes 203 and 204. A resistor R_2 is coupled between node 203 and ground, while a resistor R_1 is coupled between node 203 and back-up voltage V_B . The resistors R_1 and R_2 are configured to provide the connection 201 with a predetermined fraction of the back-up voltage V_B .

5 A resistor R_3 is coupled between the connection 202 and the primary voltage V_p . A resistor R_4 is coupled in series with capacitor C_1 between the nodes 204 and 205. A resistor R_5 is coupled between the node 204 and the node 205 (i.e., in parallel with R_4 and the capacitor C_1). The node 205 is coupled to the connection 206. A resistor R_6 is coupled between the connection 206 and the supply voltage V_S .

10 When the threshold detector 102 is in operation, the voltage V_3 is “low” if the primary voltage V_P is greater than a predetermined fraction of the back-up voltage V_B . Conversely, when the primary voltage V_P is less than the predetermined fraction of the back-up voltage V_B , then the voltage V_3 is “high.” This predetermined fraction is based on the relative values of the resistors R_1 and R_2 as well as the feedback network
15 comprising the resistors R_4 and R_5 , and the capacitor C_1 . Preferably, the resistor R_5 establishes the steady-state component of “hysteresis” while resistor R_4 and capacitor C_1 create a transient “hysteresis” effect.

FIG. 2B is a graph 210 illustrating a non-limiting example of the transient hysteresis effect created by the resistor R_4 and the capacitor C_1 . Also illustrated are
20 the settled values of the threshold created by resistor R_5 . The settled values are given as levels 215 and 216. The graph 210 has a time axis 212 and a voltage axis 211. As shown in this example, when the primary voltage V_p increases from 0V to its steady state output level 220, the threshold 214 is lowered from level 215 to level 216 after transition period t_1 . Conversely, as primary voltage V_p decreases from steady state
25 output level 220 to 0V, the threshold 214 is increased from level 216 to level 215 after transition period t_2 (where t_2 is equal to t_1). This transient hysteresis (having transition periods t_1 and t_2) protects against rapid switching between power sources. Such rapid switching may occur when the source load changes from 0% to full load.

FIG. 3 is a block diagram depicting an embodiment of the inverter 104 shown
30 in FIG. 1. The inverter 104 receives voltage V_3 and outputs voltage V_4 . The inverter 104 includes a comparator A_2 , which receives inputs via connections 301 and 302, and provides an output via connection 303. A resistor R_7 is coupled between connection 301 and ground, while a resistor R_8 is coupled from connection 301 to V_S .

This divides the voltage V_s to a lower value based on the values of resistors R_7 and R_8 . The connection 302 is coupled to the voltage V_3 . A resistor R_9 is used to pull up the voltage at connection 303 to approximately V_s when the voltage at 301 is greater than the voltage at 302. When the inverter 104 is in operation, the voltage V_4 is “low”
5 when the voltage V_3 is “high” and vice versa.

FIG. 4 is a block diagram depicting an embodiment of an inverting switch 106 (e.g., the inverting switch 106-1 or the inverting switch 106-2) shown in FIG. 1. The inverting switch 106 is coupled to voltage V_3 or voltage V_4 at connection 401, and outputs voltage V_5 at the connection 402.

10 The inverting switch 106 includes the transistors Q_1 and Q_2 , which are coupled as follows: the emitter of the transistor Q_1 is coupled to the collector of the transistor Q_2 ; the collector of the transistor Q_1 is coupled to the connection 402; a resistor R_{10} is coupled between the base of the transistor Q_1 and the connection 401; a resistor R_{12} is coupled between the base of the transistor Q_2 and the connection 401; the emitter of
15 the transistor Q_2 is coupled to ground; a capacitor C_2 is coupled between the base of the transistor Q_2 and ground; a resistor R_{11} is coupled between the collector of the transistor Q_1 and the supply voltage V_s . The transistors Q_1 and Q_2 may be, for example, bipolar npn transistors, among others.

When the inverting switch 106 is in operation, the value of the voltage at the
20 connection 401 determines whether the transistors Q_1 and Q_2 are on (i.e., conducting between their respective collectors and emitters). The transistors Q_1 and Q_2 are turned on when the voltage at the connection 401 is “high”, and vice versa. When the transistors Q_1 and Q_2 are on, the voltage V_5 is “low,” and vice versa. The capacitor C_2 causes a small delay (for example, among others, 30 milliseconds) between the
25 time that the voltage at the connection 401 transitions from “low” to “high” and the time that the transistor Q_2 turns on. A “high” to “low” transition at connection 401 immediately turns off transistor Q_1 which causes the voltage V_5 to transition “high” regardless of the turn off delay of transistor Q_2 . This “Instant on – delayed off” switching allows for a more constant voltage output of the power-switching circuit
30 100 by completely draining the old supply while the new supply is being loaded.

Resistor and capacitor values that may be used in the circuits depicted in FIGS. 2-4 may be, for example, among others, as follows:

Table 1, non-limiting examples of component values

R ₁	11 kilo-ohms
R ₂	200 kilo-ohms
R ₃	1 kilo-ohm
R ₄	51 kilo-ohms
R ₅	510 kilo-ohms
R ₆	4.7 kilo-ohms
R ₇	15 kilo-ohms
R ₈	15 kilo-ohms
R ₉	4.7 kilo-ohms
R ₁₀	300 kilo-ohms
R ₁₁	4.7 kilo-ohms
R ₁₂	300 kilo-ohms
C ₁	0.1 MF (microfarads)
C ₂	0.1 MF

Note that many alternative values for the resistors and capacitors referenced in Table 1 may be used, depending on a desired implementation.

FIG. 5 is a block diagram depicting an embodiment of a power switch 108 (e.g., the back-up power switch 108-1 or the primary power switch 108-2) shown in FIG. 1. The power switch 108 is coupled to the voltage V_P or the voltage V_B at a connection 502, and outputs the voltage V_6 at a connection 503.

The power switch 108 includes transistors Q_3 and Q_4 , which are coupled as follows: the gates of the transistors Q_3 and Q_4 are coupled to the voltage V_5 ; the drains of the transistors Q_3 and Q_4 are coupled to each other; the source of the transistor Q_3 is coupled to the connection 502; the source of the transistor Q_4 is coupled to the connection 503.

The power switch 108 is coupled to a corresponding power switch (e.g., the back-up power switch 108-1 (FIG. 1) is coupled to the primary power switch 108-2). When the power switch 108 is in operation, the voltage V_5 controls whether the voltage at the connection 502 is equal to the voltage V_6 (the voltage at the connection 503). When the voltage V_5 is high, the transistors Q_3 and Q_4 are turned on, and the voltage V_6 becomes equal to the voltage at the connection 502. Conversely, when the voltage V_5 is low, the transistors Q_3 and Q_4 are turned off, and the voltage V_6 becomes equal to the voltage provided at the connection 504 by the corresponding power switch.

FIG. 6 is a block diagram depicting an embodiment of a voltage supply circuit 600. The voltage supply circuit 600 includes diodes D_1 and D_2 . The diode D_1 is coupled between connections 601 and 603, whereas the diode D_2 is coupled between connections 602 and 603. The voltages V_P and V_B are provided as inputs to the voltage supply circuit 600 at the connections 601 and 602, respectively. The voltage supply circuit 600 outputs the voltage V_S at the connection 603. The voltage V_S is equal to the voltage V_B or the voltage V_P , whichever is higher. Examples of voltage supplies that may be used to provide the voltage V_B or the voltage V_P include, for example, among others, a battery, an AC to DC converter, or a DC/DC converter.

FIG. 7 is a flow chart depicting a method 700 according to one embodiment of the invention. In step 701, a primary voltage is provided to a load. Then, a drop in the primary voltage below a predetermined threshold is detected, as indicated in step 702. The drop in primary voltage may, for example, be detected using a circuit that is configured in the same or similar manner as the threshold detector 102 (FIG. 2A).

Responsive to the drop in the primary voltage, a first circuit having at least one transistor (e.g., connected in-line) is used to provide a back-up voltage to the load, as indicated in step 703. In addition, a second circuit having at least one transistor is used to disconnect the primary voltage from the load, as indicated in step 704. The first and the second circuits used for implementing steps 703 and 704, respectively, may, for example, each be configured in the same or similar manner as the power switch 108 shown in FIG. 5.

In an alternative implementation, the steps depicted in FIG. 7 may be executed out of order from that shown or discussed, including substantially concurrently or in reverse order, as would be understood by those of ordinary skill in the art. For example, steps 703 and 704 may be executed substantially concurrently. Furthermore, the scope of the invention includes methods having fewer or additional steps than shown in FIG. 7.

It should be emphasized that the above-described embodiments of the present invention are merely possible examples, among others, of the implementations, setting forth a clear understanding of the principles of the invention. Many variations and modifications may be made to the above-described embodiments of the invention without departing substantially from the principles of the invention. All such modifications and variations are intended to be included herein within the scope of the

disclosure and present invention and protected by the following claims. In addition, the scope of the present invention includes embodying the functionality of the preferred embodiments of the present invention in logic embodied in hardware and/or software-configured mediums.